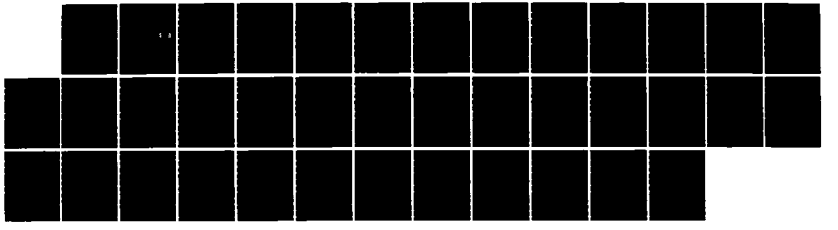
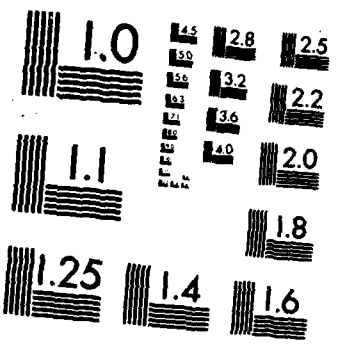
AD-A173 176 TECHNIQUES OF MICROPROCESSOR TESTING AND SEU (SINGLE EVENT UPSET)-RATE PR..(U) AEROSPACE CORP EL SEGUNDO CA SPACE SCIENCES LAB R KOGA ET AL. 15 AUG 86 1/1

UNCLASSIFIED TR-0086(6940-05)-20 SD-TR-86-52 F/G 9/2 NL





REPORT SD-TR-86-52

Techniques of Microprocessor Testing and SEU-Rate Prediction

Prepared by

R. KOGA, W. A. KOLASINSKI, and M. T. MARRA
Space Sciences Laboratory
Laboratory Operations
The Aerospace Corporation
El Segundo, CA 90245

15 August 1986

Prepared for

SPACE DIVISION
AIR FORCE SYSTEMS COMMAND
Los Angeles Air Force Station
P.O. Box 92960, Worldway Postal Center
Los Angeles, CA 90009-2960

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER SD-TR-86-52	2. GOVT ACCESSION NO. AD-A173 176	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) TECHNIQUES OF MICROPROCESSOR TESTING AND SEU-RATE PREDICTION		5. TYPE OF REPORT & PERIOD COVERED 6. PERFORMING ORG. REPORT NUMBER TR-0086(6940-05)-20
7. AUTHOR(s) Rokutaro Koga, Wojciech A. Kolasinski, and Michael T. Marra		8. CONTRACT OR GRANT NUMBER(s) F04701-85-C-0086
9. PERFORMING ORGANIZATION NAME AND ADDRESS The Aerospace Corporation El Segundo, Calif. 90245		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Space Division Los Angeles Air Force Station Los Angeles, Calif. 90009-2960		12. REPORT DATE 15 August 1986 13. NUMBER OF PAGES 35
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Micropressor Testing
Single Event Upset
Radiation Hardness

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Several different approaches have been used in the past to assess the vulnerability of microprocessors to SEU. In this report we discuss the advantages and disadvantages of each of these test methods, and address the question of how the microprocessor test results can be used to estimate upset rate in space. Finally, as an application of the above techniques, we present the test results and predicted upset rates in synchronous orbit for a selected group of microprocessors.

DD FORM 1473 (FACSIMILE)

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

PREFACE

The authors wish to express their appreciation to The Aerospace Corporation personnel for assisting with the experiments. The authors are also grateful to the SEU test collaborators from Harris, McDonnell Douglas, NWSC-Crane, Analex, NASA GSFC, and Sandia, as well as the entire accelerator staff at IUCF, HHIRF, 88-in. Cyclotron (LBL), and Bevalac (LBL), who made the SEU testing possible.

CONTENTS

FIGURES

TABLES

I. INTRODUCTION

A microprocessor has been studied for its vulnerability against cosmic ray induced errors such as single event upset (SEU) and latch-up. Earlier reports on the observation[1,2,3,4] of SEU in microprocessors were followed by several mentions of test results in the SEU summary format.[5,6] As the needs for advanced control and computing capabilities increase in satellite applications, a wide range of microprocessors as well as other microcircuits will be considered for use. Therefore, the ability to predict rates of upset of these devices in space is becoming an important factor. In this report we would like to limit our attention to microprocessors (including bit slice processors), report on the various SEU test techniques oriented towards predicting upset rate in space, and present some predictions based on recently conducted tests.

The prediction of a microprocessor SEU rate in space requires both the laboratory SEU test data and some circuit analysis, in addition to the general knowledge of program execution procedures. In the future, circuit simulation alone can be used for the upset rate determination but, as yet, simulation techniques have not reached the critical level of maturity where no laboratory-test confirmation is needed. Each confirmation refines the circuit-simulation technique, and eventually the latter may become the chief means of predicting the upset rate. Thus, the existence of a published extensive and readily accessible data base of experimental SEU test results is extremely valuable in the process of evolution of predictive techniques based on circuit simulation and device modeling. Extensive data bases already have been published for predicting SEU rates of RAMs and relatively simple logic devices, and their use is fairly routine. In contrast, microprocessor data bases are just beginning to emerge, and it is not entirely clear how one should use what little there is. Microprocessor SEU test data need to be presented differently from those pertaining to simple latches or RAMs, where the cross-section vs LET curve has a simple meaning and is readily usable for estimating the upset rate in space. In order to obtain comparable data for a microprocessor,

it is essential to analyze carefully various possible test methods and their implications regarding the desirable device characterization.

II. MICROPROCESSOR TEST METHODS

In devising a test method for a microprocessor, we begin by examining all possible functional elements. If we can test the SEU vulnerability of each functional element, the combined rate of SEU in space can be estimated from the program execution pattern. This "macroscopic" (functional element as opposed to individual circuit) testing of many functional elements can be accomplished "externally" using the standard instruction sets (i.e., there is no need to obtain test device circuits especially fabricated for microscopic SEU testing.) It should be remembered that macroscopic testing may be the only available means of ascertaining the SEU rate of a commercially available microprocessor, since neither a detailed knowledge of the device nor test circuits will in general be readily obtainable.

While testing various microcircuits, we have considered and developed five methods of microprocessor testing. After briefly defining these below, we will introduce each one in some detail with the help of examples of devices actually tested. The methods we will consider are:

1. Self-testing Single Computer Method: a microprocessor can be tested in a simple computer configuration, e.g., single board computer. The processor "self-tests" and the result of the self-test can be visually recognized either by a CRT displayed output pattern or even by a simple LED.

2. Controller Assisted, Single Computer Method: an external controller interrogates the operation of the microprocessor under test by comparing its outputs with the "true" values stored in an external memory table.

3. Controller Assisted, Golden Chip Method: an external controller compares the outputs of the microprocessor under test with the outputs of a "standard" microprocessor (golden chip) operation under the same program. In the above three methods the microprocessor under test automatically fetches the instructions stored in memory (RAM or ROM) whenever it requires them.

4. Controller Dominated, Single Computer Method: it is possible for the controller to "take over" the function of the simple computer memory by introducing instructions whenever the microprocessor under test requires them. Here the instructions are "force-fed," and the microprocessor under test effectively single-steps through the given program sequentially. The same controller interrogates the outputs of each step.

5. Controller Dominated, Golden Chip Method: this is another single-step method. The interrogation of upsets consists of comparing the outputs of the microprocessor under test and those of a "standard" microprocessor (golden chip) operating under the same program. The controller stores the error data.

In all methods, except for the first one, the speed of the operation is limited by that of the controller during the handshake. The controller is usually a micro- or mini-computer which requires tens of microseconds to collect and store data. Therefore, the clock frequency of a DUT must be interrupted while the controller collects upset data. A concept of "average clock frequency" is introduced to specify the average clock rate during the test period. A comparison (pros and cons) of the five test methods is made in Table 1.

Table 1. A Comparison of the Five Test Methods

TEST METHODS / TRADE-OFF CRITERIA	SELF-TESTING SINGLE COMPUTER	CONTROLLER ASSISTED		CONTROLLER DOMINATED	
		SINGLE COMPUTER	"GOLDEN CHIP"	SINGLE COMPUTER	"GOLDEN CHIP"
EFFECTIVE CLOCK FREQUENCY	HIGH	MEDIUM	MEDIUM	LOW (< 10 kHz)	LOW (< 10 kHz)
INDIVIDUAL ELEMENT TESTABILITY	LOW	HIGH	HIGH	HIGH	HIGH
ERROR-TABLE STRUCTURE/ DATA DISPLAY	SIMPLE	COMPLEX	COMPLEX	COMPLEX	COMPLEX
TEST PREPARATION LEAD-TIME	SHORT	MEDIUM	MEDIUM	MEDIUM	LONG
DEVICES TESTED	1802 SA3000	1802, 6800 80C86, 8X300 MD2815, 8X305 SA3000	9900 9989 F9445	2901	Z80 NSC800

III. ILLUSTRATION OF TEST METHODS: DETAILED EXAMPLES

A. 4-BIT SLICE PROCESSOR (2901) (METHOD 4)

The block diagram of the device is shown in Figure 1a. The 2901 is a 4-bit slice processor. It is essentially a static device, and the clock can be operated at any frequency up to 15 MHz. The RAM section (16 × 4 bit), a Q register, and A and B port latches (2 × 4 bit) are the only memory elements, and all were tested for SEU. The ALU is used each time the data is placed in the Q register or the RAM. Therefore, a change in the writing frequency alters the degree of the ALU circuit involvement and enables us to measure the SEU vulnerability of ALU.

This device is much like a SRAM (or D flip-flop) from the standpoint of SEU testing. We used a simple version of test method no. 4, in which the test clock frequency is limited to about 10 kHz.

The software instruction sequence of our SEU test procedure is shown in Figure 2. The clock pulse controls the A- and B- latches as well as the WRITE RAM process. The clock line must be kept "high" during the read cycle in order to minimize errors associated with corrections during data analysis. The clock line was "low" for one waiting cycle, and "high" for the next cycle. This process was repeated many times until a statistically significant number of upsets were obtained.

There are many versions of the 2901, fabricated in TTL, ECL, and CMOS with varying vulnerabilities to SEU. The test results of these devices are presented and discussed in the following section, along with the results for the same device type tested earlier using a simpler version of test method no. 5.*

The 2901 processor is not a full microprocessor, and it cannot "run by itself." Therefore, one can test it only with method nos. 4 or 5. We selected method no. 4 because the test preparation time was relatively short and because observation of the RAM, port latches, and Q register could be readily implemented.

---

*K. L. Wahlin, private communication.

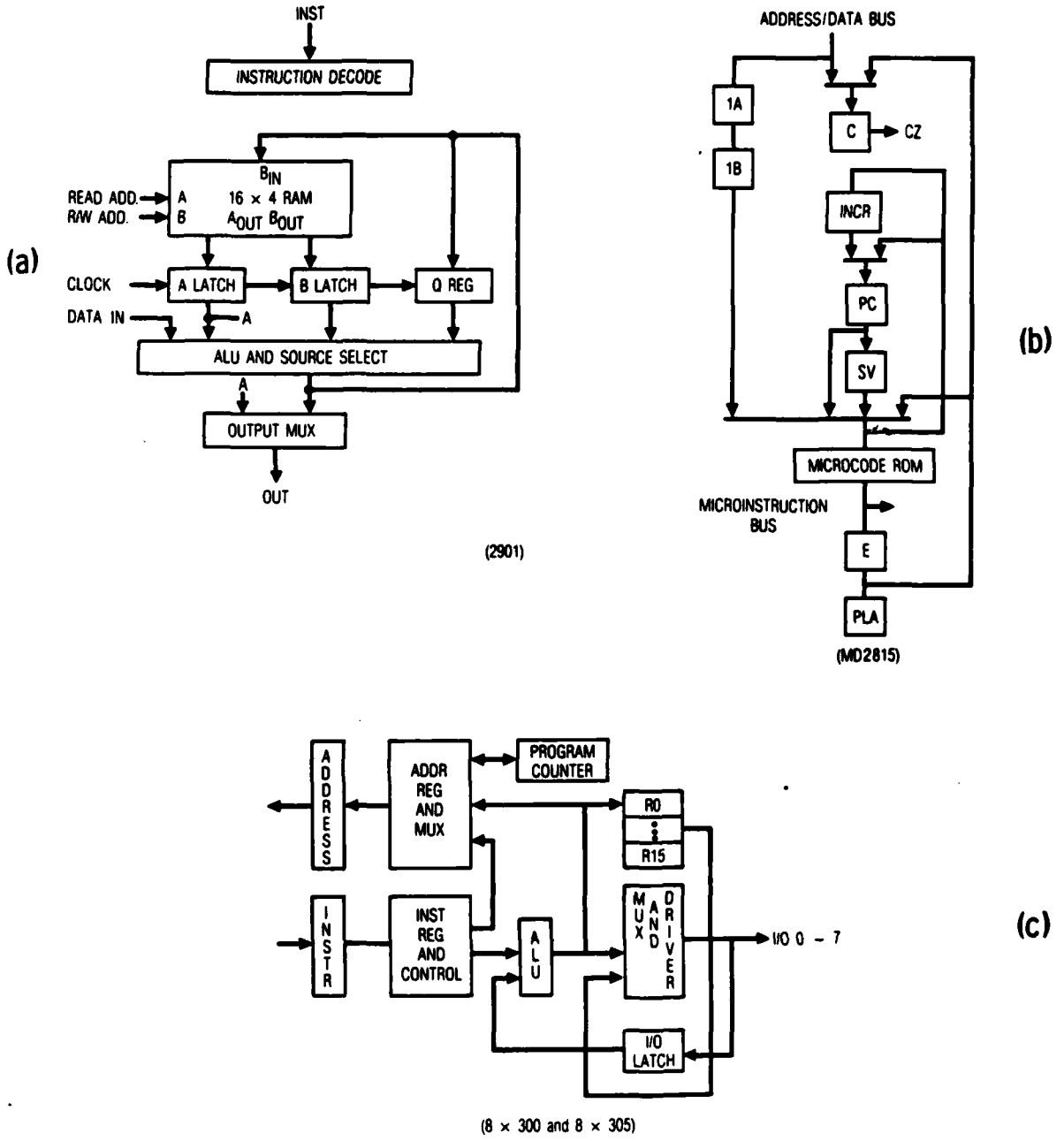


Figure 1. Functional Elements of Microprocessors. (a) 2901, (b) MD2815, and (c) 8 × 300 and 8 × 305.

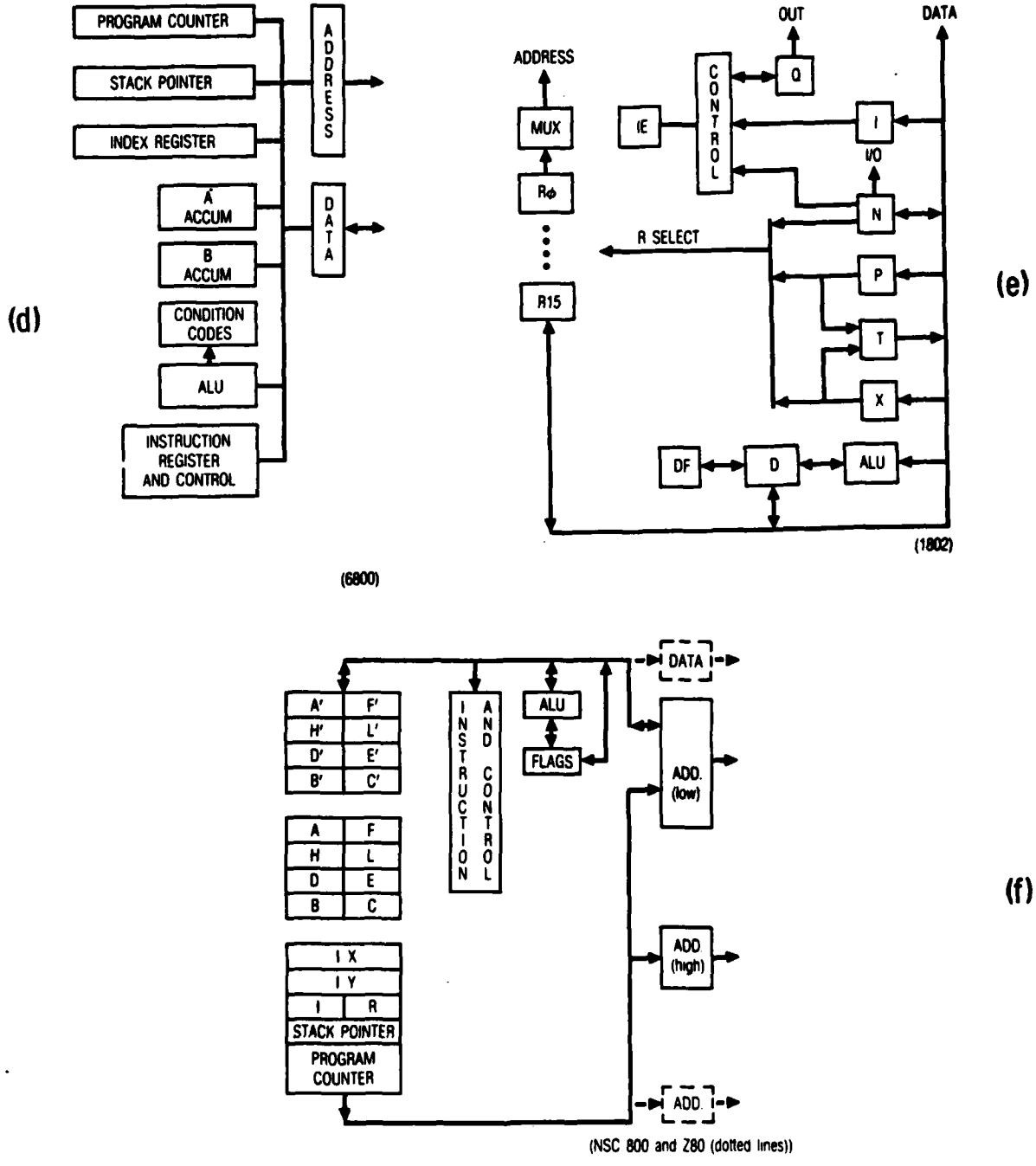


Figure 1. Functional Elements of Microprocessors. (d) M6800, (e) 1802, and (f) NSC800 and Z-80.

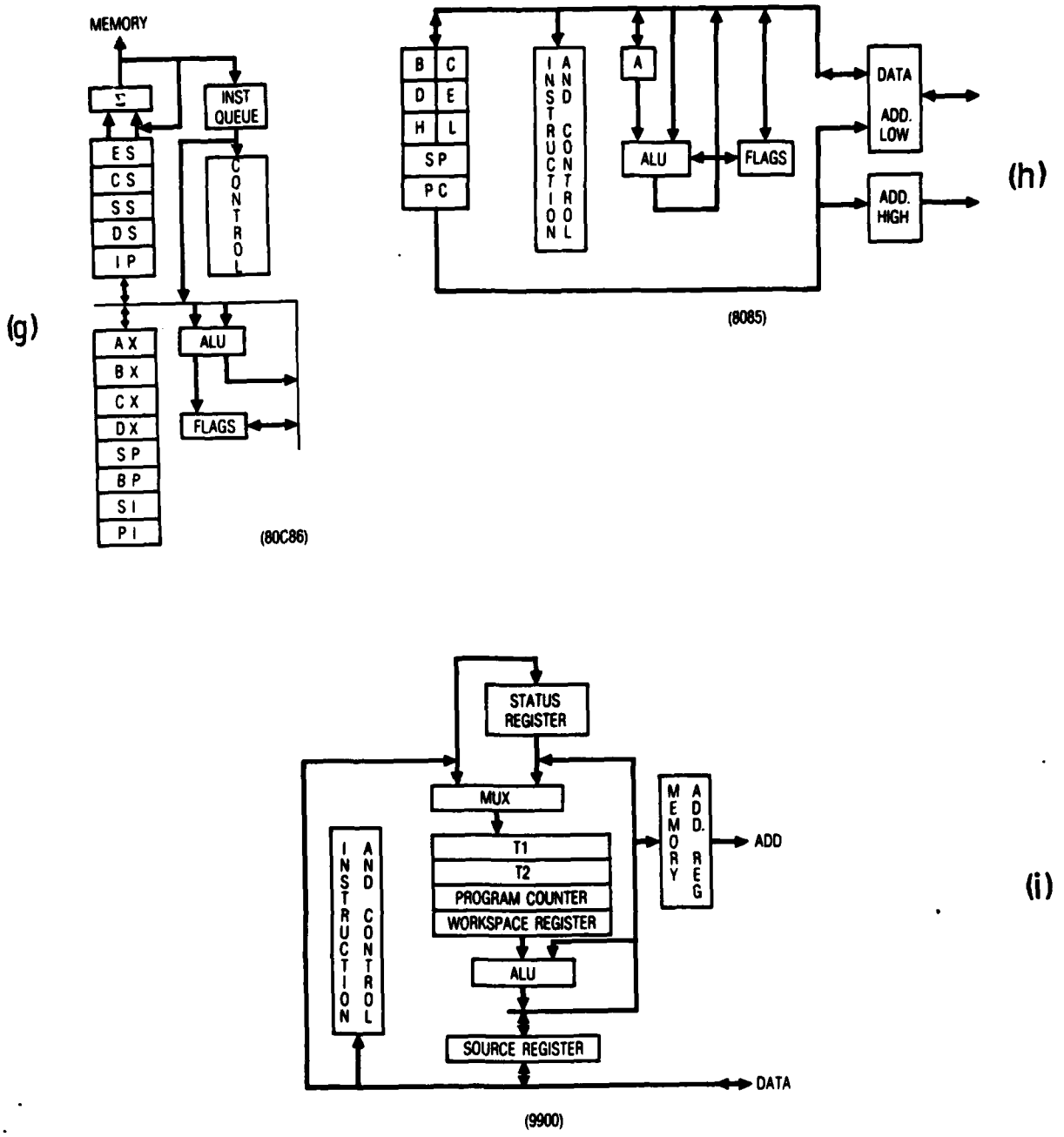


Figure 1. Functional Elements of Microprocessors. (g) 80C86, (h) 8085, and (i) 9900.

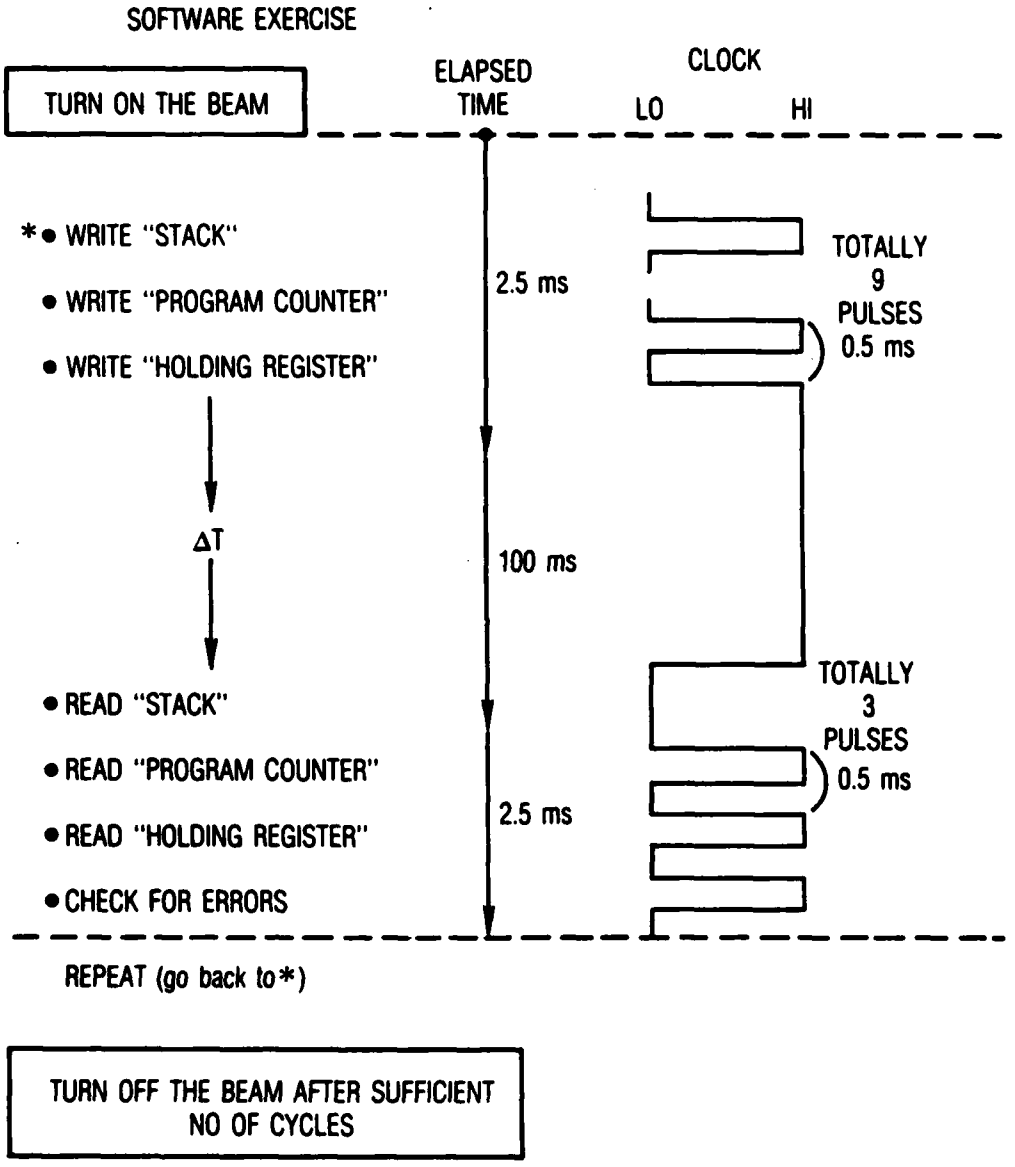


Figure 2. The "2901" Test Procedure

B. 16-BIT MD2815 PROCESSOR (METHOD 4)

The MD2815 control unit (CU) of the McDonnell Douglas' 1750A microprocessor (CMOS/SOS) contains the microprogram ROM and the next-instruction logic to generate the next-microprogram addresses in the sequential operation of the microprocessor as shown in Figure 1b. The next-instruction logic consists of a microprogram counter (PC), an incrementer (INCR), a register to save the program counter (SV), an iteration counter (C), and an instruction decode logic. The system timers IA and IB are a part of the interrupt handing logic. This device, just like the 2901, is a building block of a microprocessor, and the test procedure used in the 2901 was also applicable for MD2815. We used test method no. 4 in order to interrogate the PC register and the 1K × 40-bit microcode ROM. The reason behind choosing this method is the same as that stated in the previous section.

C. 8-BIT MICROCONTROLLERS AND MICROPROCESSORS (METHODS 1, 2, AND 5)

The 8X300 and 8X305 (manufactured by Signetics in full ECL and LS TTL for I/O) are "old" but still very useful processors. The 8X300 was introduced in 1968 and the 8X305 in 1972, and both devices have the same functional elements as shown in Figure 1c. These are the sixteen 8-bit data registers, one 13-bit program counter, one 13-bit address register, one 16-bit instruction register, one 8-bit I/O latch, the ALU, and the control and timing logic circuits. The devices lack the complexity of the present level microprocessor, and therefore they are called microcontrollers. The clock frequency can be varied from DC to 10 MHz. Since operation over the design range of frequencies was an important consideration, we used test method no. 2. During the test, 16 data registers, the program counter, and the ALU were interrogated for upset, since these were representative of the full set of functional elements of the device.

The 6800 NMOS microprocessor (Motorola) consists of several functional groups such as two 8-bit accumulators (A and B), one 16-bit index register (IX), one 16-bit stack pointer (SP), one 16-bit program counter (PC), one 6-bit condition code register (CCR), ALU, and the control logic as shown in Figure 1d. The clock frequency must be kept between 0.1 and 2.0 MHz. Thus,

again we used method 2 to check A, B, IX, SP, PC, CCR, and ALU elements for SEU.

The 1802 microprocessor was designed over a decade ago, and the radiation hardened version of 1802 has been used in spacecraft applications where the radiation environment is particularly severe such as that in case of Galileo. There is no minimum frequency requirement (the system can be held in a static mode), and maximum clock frequency is about 6 MHz. The system has one 8-bit data register (accumulator D), one 1-bit data-flag (DF), sixteen scratch resisters (R), one 4-bit program counter selector (P), one 4-bit stack pointer selector (X), one 4-bit high order instruction bits holder (N), one 4-bit low order instruction bits holder (I), one 8-bit old -X and -P holder (T), one 1-bit interrupt enable flag (IE), one output flip-flop (Q), one ALU, and the control logic as shown in Figure 1e. We used method no. 2 to test 15 R's, D, N, Q, and ALU. In addition, we employed method no. 1 to check operation with a set of simple but well mixed instructions.

While testing the above devices under method no. 2, we encountered a problem connected with an occasional SEU occurring either in the instruction register or in the program counter. Following such an event, the single board computer would sometimes lose track of itself, and a catastrophic failure would result. To circumvent this type of failure, we installed a watchdog timer which would log the failures and re-initialize the microcomputer. The total number of such failures yielded the combined error rate of PC and the instruction register.

An alternative way to handle the recovery from catastrophic failure is to use method nos. 4 or 5. While testing the following two 8-bit microprocessors, we employed method no. 5. Space does not permit a description of the many unique features of this method. A detailed example of its application is provided in Ref. 7.

Both the Z80 (manufactured by Zilog in the NMOS technology) and the NSC800 (manufactured by National in the CMOS technology) have identical instruction sets. A block diagram of NSC800, which also represents the Z80, is shown in Figure 1f. The microprocessors consist of eight 16-bit register

arrays (AFHLDEBCA'F'H'L'D'E'B'C'), two index registers (IX, IY), two 8-bit vectors (I, R), one stack pointer, one program counter, one 8-bit instruction register, one 6-bit flag, ALU, and the control logic.

The clock frequency of NSC800 can be varied from 16 kHz to 3 MHz, whereas Z80 has the lower limit of 0.1 MHz and the upper limit of 3.0 MHz. (The clock for NSC800 can be stopped without losing any data only at some certain phase.)

D. 16-BIT MICROPROCESSOR (METHOD 2)

The 80C86 microprocessor, manufactured by Harris in CMOS technology (the mask number was 1750), was tested using test method no. 2. All internal registers, counters, and latches are of static design. The clock frequency can vary from DC to 5 MHz. It functionally consists of four 16-bit segment-register-files (code segment-CS, stack segment-SS, data segment-DS, extra segment-ES), four 16-bit general registers (accumulator-AX, base-BX, count-CX, data-DX), four 16-bit special registers (stack pointer-SP, base point-BP, source index-SI, destination index-DI), one 16-bit instruction pointer (IP), one 16-bit status flag (FLAGs), ALU, and the control and timing logic as shown in Figure 1g. Both CMOS/EPI and CMOS/Bulk versions were tested using method no. 2. We needed to test the device in a reasonably short time scale. Therefore, we chose test method no. 2.

E. OTHER DEVICES

The block diagram of 8085 and 9900 are shown in Figure 1h, and 1i, respectively. The Sandia verion of 8085 (SA3000) was tested by methods no. 1 and 2, and 9900 (also 9989) was tested by test method no. 3.[2]

All five test methods have been used since 1980. Method 2 may in principle be replaced by test method 3 or vice versa. However, each test method provides some unique features, and it will have its own place in the SUE testing.

IV. METHODS OF UPSET-RATE PREDICTIONS

There are three stages in the process of estimating the upset rate of a microprocessor. First, we need to select an appropriate test method, using selection criteria such as microprocessor architecture, operating speed, instruction formats, circuit design, and application software. Second, it is necessary to deduce the SEU cross-section as a function of LET for various registers and any other elements (using appropriate ground-test procedures and microprocessor element utilization factors during software executions). Finally, using an appropriate physical device model, we can combine data from step 2 with a radiation environmental model to compute upset rate in that environment.[8,9]

While the use of a cross-section vs LET curve to predict the upset rate of a RAM is quite straightforward, matters are not nearly as simple in the case of microprocessors. A considerable amount of analysis is required to come up with a cross-section curve which will yield realistic upset-rate predictions for a microprocessor.

For a bit slice processor (e.g., Figure 1a), a typical micro-instruction should be taken into consideration in order to estimate the number of "live and relevant" registers. By "live and relavant" register, we mean those registers whose SEU will cause observable errors during the relavant program execution. For example, if addition of two numbers were carried out soon after loading of the two numbers, only two registers and the ALU would be vulnerable during the time period. Here, we can come up with a model of typical duty cycle for the vulnerability through Monte Carlo simulation using a set of instructions, or analysis of vulnerability using the actual existing applications program. A simple first order model using a less sophisticated approximation can always be applied. In the past, for example, the average SEU rate per bit based on upset cross-sections measured for the various registers was simply multiplied by the number of total bits to estimate the device-wise SEU rate.[2] This may over-estimate the device upset rate by as much as one order of magnitude.

In the more standard microprocessor, the classification of various functional elements into the "live and relevant group" as a function of time can be always accomplished in similar manner. However, a first order approximation can be done quickly knowing that the program counter and the instruction decoder are continuously being used, whereas the use of other elements is less frequent. More advanced microprocessors such as the 80C86 "look ahead" to the next instructions and even hold several bytes of the instruction stream within the processor. In these devices, consideration of the duty cycle alone can provide a first order approximation of the upset rate of the whole device.

V. UPSET-RATE PREDICTION RESULTS

In this section we present detailed results for the three devices discussed above. Several versions of the bit-slice microprocessor are considered. The 6800 and 80C86 microprocessors were chosen as examples of "old" and "new" microprocessor types, respectively. Additional test results and upset rates for other recently tested devices are also shown in Table 2.

A. 4-BIT SLICE PROCESSOR (2901)

We have tested commercially available Am2901's manufactured by AMD. These are presently available in B (low power Schottky) and C (mostly ECL with some low power Schottky) versions. The SEU vulnerability of the RAM, the Q register, and the port latches for Am2901B are shown in Figures 3a, 3b, and 3c, respectively. Similar curves for Am2901C are shown in Figures 4a, 4b, and 4c, respectively.

The SEU rate of the device was not dependent on the clock frequency, which agrees with an earlier observation on a NMOS microprocessor.[1] Also, the errors arising from the ALU were insignificant in this device. The RAM cross-sections were mainly taken from unaddressed storage elements. The probability of upset during the addressed elements has been reported to be lower.[10] However, at most only one out of 16 can be addressed, and so this fact does not affect the total response of the device. The bit pattern used to simulate a common program was 50% "1" and 50% "0."

It was reported earlier that the average Krypton or Argon fluence for one upset per Am2901B was a few hundred particles/cm^2.[4] Our results agree with that value. However, our interest is to produce the upset rate in space due to cosmic rays, and not to be content with measuring the laboratory upset rate only. Now, how can we relate the measured cross sections to the upset rate in space? The answer lies in the software programming of Am2901B. In order to predict an upset rate in space from the above data, a general programming knowledge of the microprocessor is needed.

Table 2. SEU Test Results and Upset Predictions

Device I.D.	Mfr	Technology	Test Method	Tested Elements	Test Facility	Test Org.*	Composite or Effective LET(th.)**	Cross-s.***	SEU **** (upset/device-day)
1802	RCA	CMOS	1,2	ACC,16 REGs,ALU	88in(LBL)	A(84)	>80	<5.0E-7	<1.0E-8
1802	SNL	CMOS	1,2	ACC,16 REGs,ALU	88in(LBL)	A(84)	>80	<5.0E-7	<1.0E-8
MD2015	MDA	CMOS/SOS	2	MICROCODE ROM,PC	88in(LBL)	A,M(84)	>120	<6.0E-7	<2.0E-9
Am2901B	AMD	LS TTL	4	RAM,2 LATCHEs,Q-REG,ALU	88in(LBL)	A(84)	4	3.0E-4	9.0E-3
Am2901C	AMD	ECL	4	RAM,2 LATCHEs,Q-REG,ALU	88in(LBL)	A(84)	8	5.0E-4	4.0E-3
SA2901	SNL	CMOS;8 k	4	RAM,2 LATCHEs,Q-REG,ALU	88in(LBL)	A(84,85)			
SA2901	SNL	CMOS;80k	4	RAM,2 LATCHEs,Q-REG,ALU	88in(LBL)	A(84,85)	>160	<1.0E-10	<2.0E-12
SA3000	SNL	CMOS	1,2		88in(LBL)	A,S(83)	40(+7.5)	5.0E-7	1.6E-7
M6800	MOT	NMOS	2	2 ACCs,IX,PC,SP,CCR,ALU	88in(LBL)	A(84)	7	3.0E-4	3.1E-3
80C86	HAR	CMOS	2	ACC,11 REG,PC,F,ALU	88in(LBL)	A,H(84)	11	6.0E-2	2.5E-1
80C86	HAR	CMOS/EPI	2	ACC,11 REG,PC,F,ALU	88in(LBL)	A,H(84)	11	6.0E-2	2.5E-1
F9445	FSC	IIIL	3		88in(LBL)	A,(84)	20	1.5E-4	1.9E-4
9900	TI	IIL	3		88in(LBL)	A,C(84)			
9989	TI	IIL	3		88in(LBL)	A,(84)	>25	2.5E-4	

* A:Aerospace,C:NNSC-Crane,H:Harris,M:MDAC,S:Sandia
** MeV/(mg/sq.cm)
*** sq.cm/device
**** Model dependent results at the Syosynchronous orbit(1JUL85)

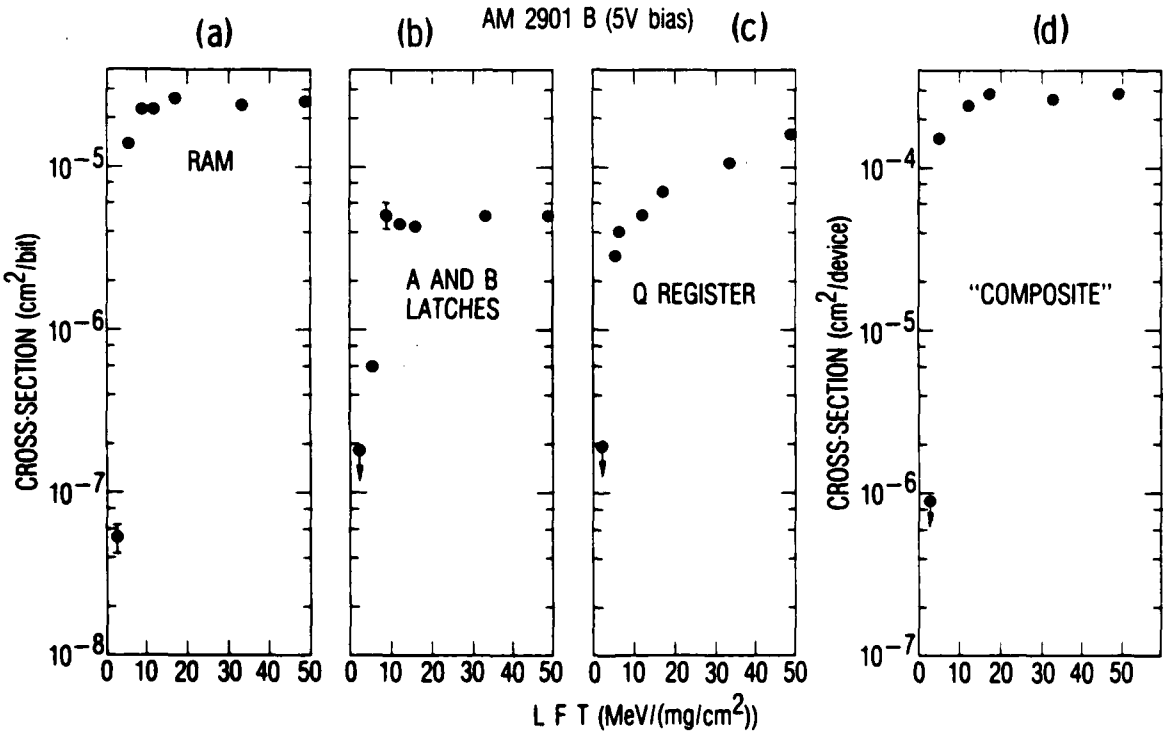


Figure 3. The Cyclotron Test Results of 2901B

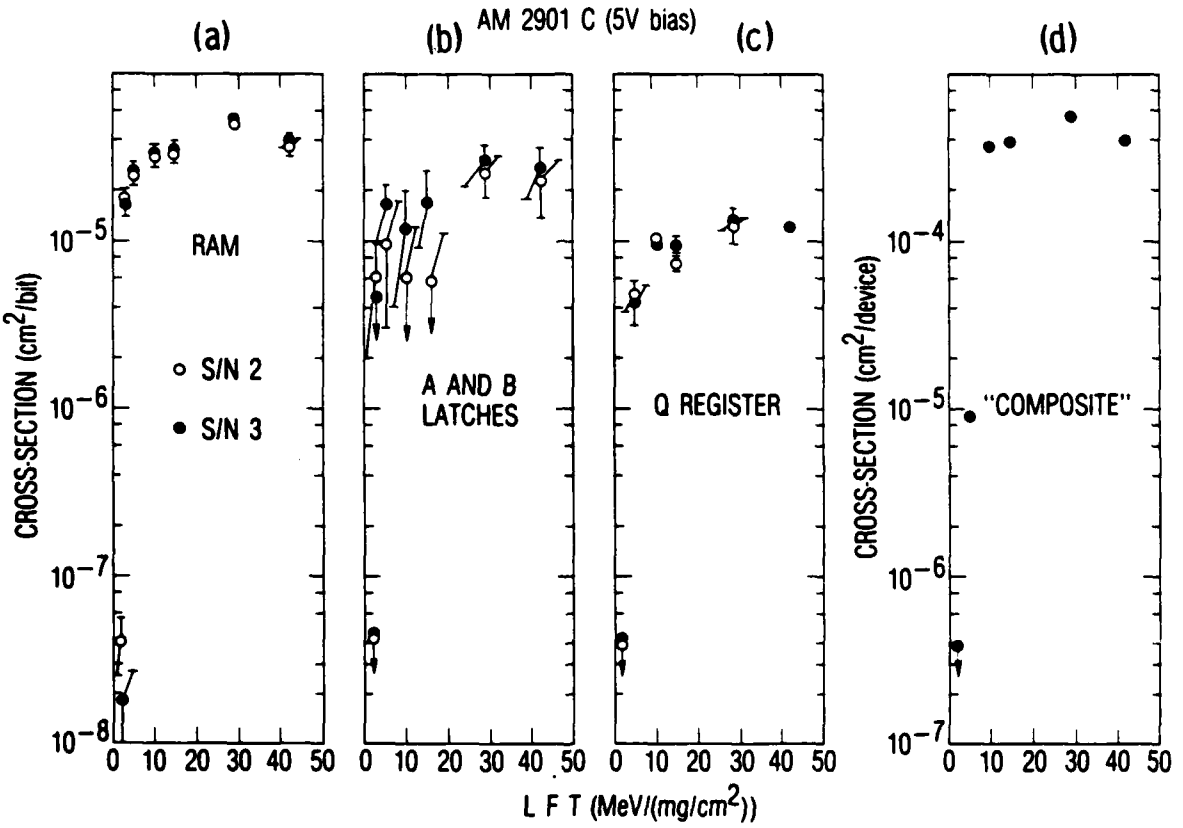


Figure 4. The Cyclotron Test Results of 2901C

For example, one can say that about 1/2 of the 2901B instruction set deals with the manipulation of a stored value in the RAM and a value in the Q register (e.g., ADD (Q) and (RAM address 1) before storing the result in (RAM address 2)). In this mode of operation, we use the Q register and only 2/16 of the RAM space. The rest of the instruction set in this model deals with two numbers in the RAM. Here, we do not use the Q register. Then, on the average, the programming duty cycle of the Q register is 50%, whereas that of the RAM is 16%. Within the program, an SEU error in the port latches has little effect on the total upset rate. Therefore, we can calculate the functional upset cross section for Am2901B in this typical program by using the three individual cross-section curves as shown in Figure 3d (composite curve). Using the curve in the figure, we can calculate the upset rate in space with the methods described by Petersen or Adams.[8,9] It must be remembered that this result is based on one particular mix of program routines. A similar calculation can be made given another mix of programming routines. However, without the help of the three curves as shown in Figure 3a, b, and c, it would have been impossible to proceed. Also, if one were to include 100% of RAM and 100% of the Q register, the upset prediction would be overestimated by a factor of about 6.

The Sandia National Laboratory has produced a CMOS version of 2901. Cross coupled resistors of approximately 80K ohm were used in critical cells. Since the device was inherently very strong against SEU, we used 300 MeV krypton and 451 MeV xenon ions at the 88-inch cyclotron facility for extensive SEU testing. The results are summarized in Table 2.

The krypton and zenon ions used in this test have become available only recently. The electron cyclotron resonance (ECR) heavy-ion source was first successfully used for SEU and latch-up testing at the 88-inch cyclotron facility (LBL). The ECR source enables us to utilize higher energy and higher Z ions for testing. The summary of representative ions presently available at the 88-inch cyclotron facility is shown in Table 3.

Table 3. ECR Ion Beams Used in SEU Testing

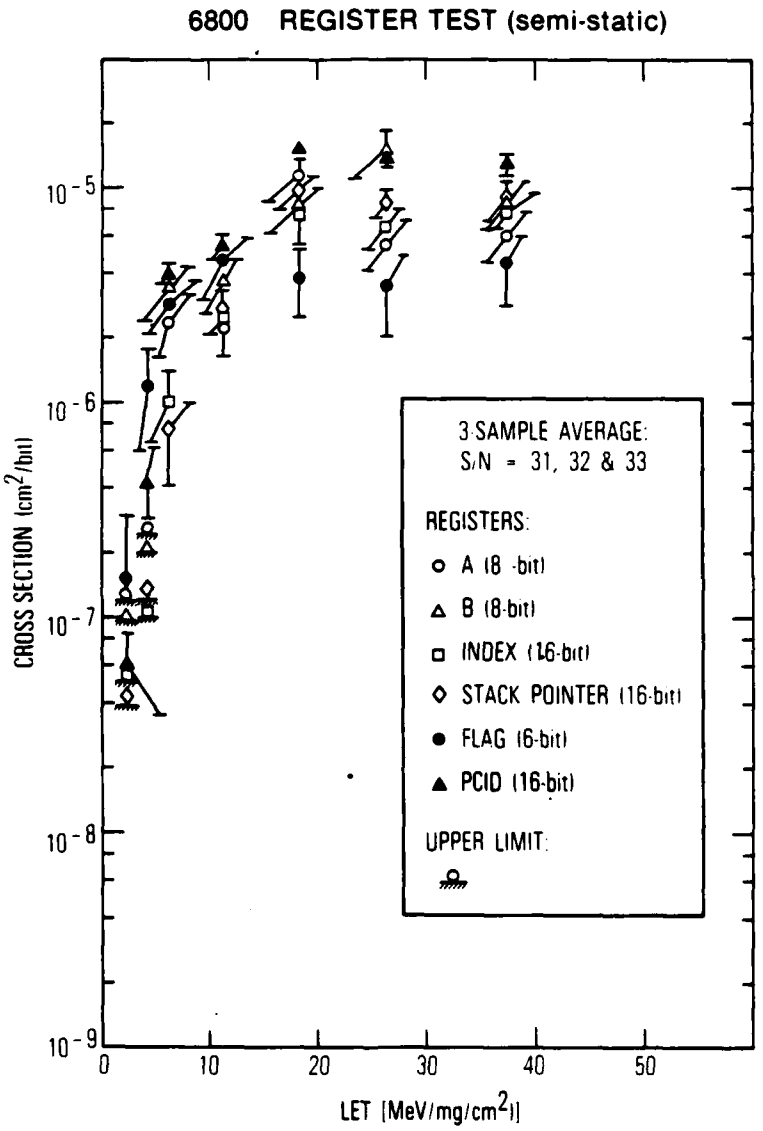
Element	Atomic No.	Mass No.	Energy (MeV)	dE/dX (MeV/ mg/cm^2)	Range (μ)	Accelerator Facility	Beam Duty Cycle
N	7	15	68	3.0	66	88in Cyc.	1 %
Ne	10	20	80	6.0	45	88in Cyc.	1 %
Ar	18	40	163	15.0	41	88in Cyc.	1 %
Kr	36	84	300	40.7	38	88in Cyc.	1 %
Xe	54	129	451	60.2	43	88in Cyc.	1 %

B. M6800 MICROPROCESSOR

The device is fabricated by Motorola in NMOS. We used three test programs under test method no 2: (1) The first one tested A(8-bit), B(8-bit), X(16-bit), SP(16-bit), and F(6-bit) registers (see Figure 1d). The X-register, for example, was tested by placing a known pattern on it during the exposure, and reading it some time later to check for errors. Over the years, this type of interrogation technique has been used in testing RAMs in a static condition. In this test the program counter and the instruction register are continuously exercised while the registers are static. Hence, this test is called "semi-static." We summed all errors resulting in catastrophic failure, such as an unexpected jump of the program counter, and termed them the program counter and/or instruction decoder, "PCID," error. The above results, as well as the semi-static upsets, are shown in Figure 5a.

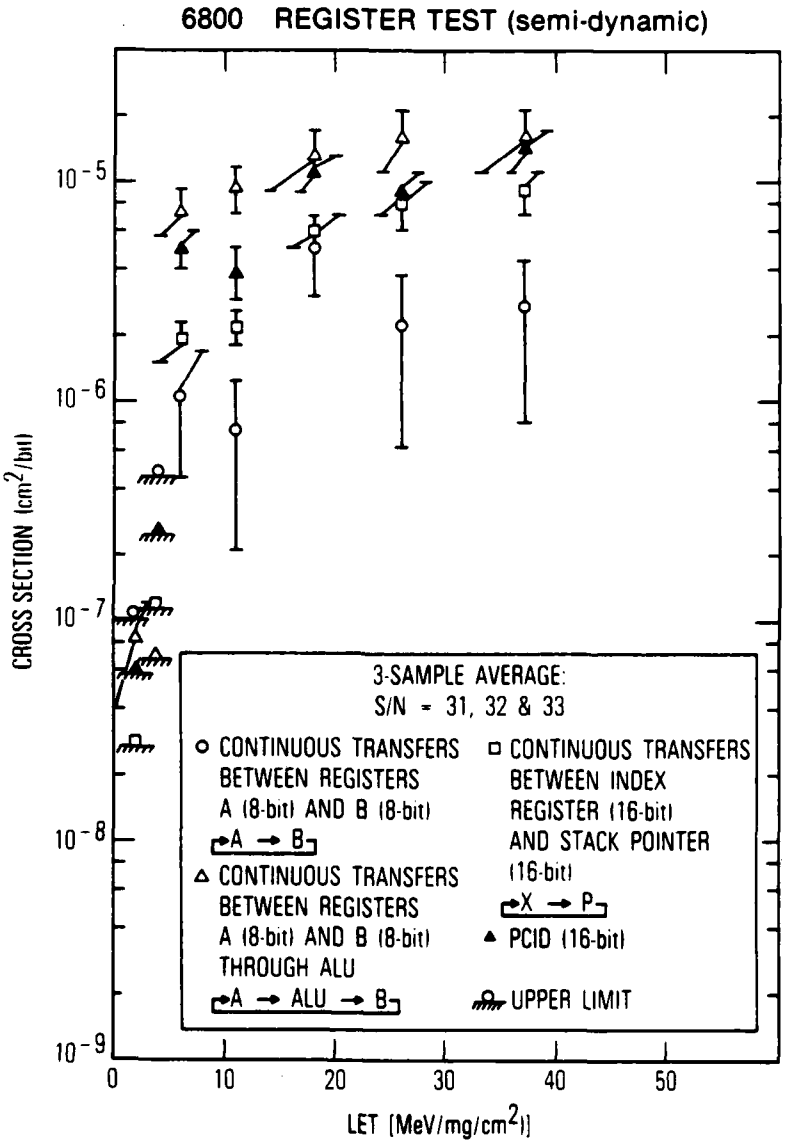
Another program sequence to test the microprocessor involved writing a pattern on the x-register and transferring the contents of the x-register to the SP register, then back to the x-register, etc., for a given time, in order to observe the bit error. The microprocessor was programmed to perform the transfer task only during exposure to beam. In this fashion, we tested A, B, X, and SP. In some cases the ALU was placed in the program loop to test the vulnerability of the ALU section. As before, we encountered errors in the "PCID" category. The results are shown in Figure 5b. We call this test "semi-dynamic." The cross-section vs LET curve of the "PCID" in the semi-static test overlaps almost identically with that of the "PCID" curve in the semi-dynamic test results. This result was expected, since they are essentially the same exercise as far as the program counter and the instruction decoder are concerned.

The vulnerability of A, B, X, and SP registers did not depend very much on the semi-static and semi-dynamic nature of the test program. One possible exception is that accumulators A and B exhibited a high resistance against SEU during the semi-dynamic test and not in the semi-static test.



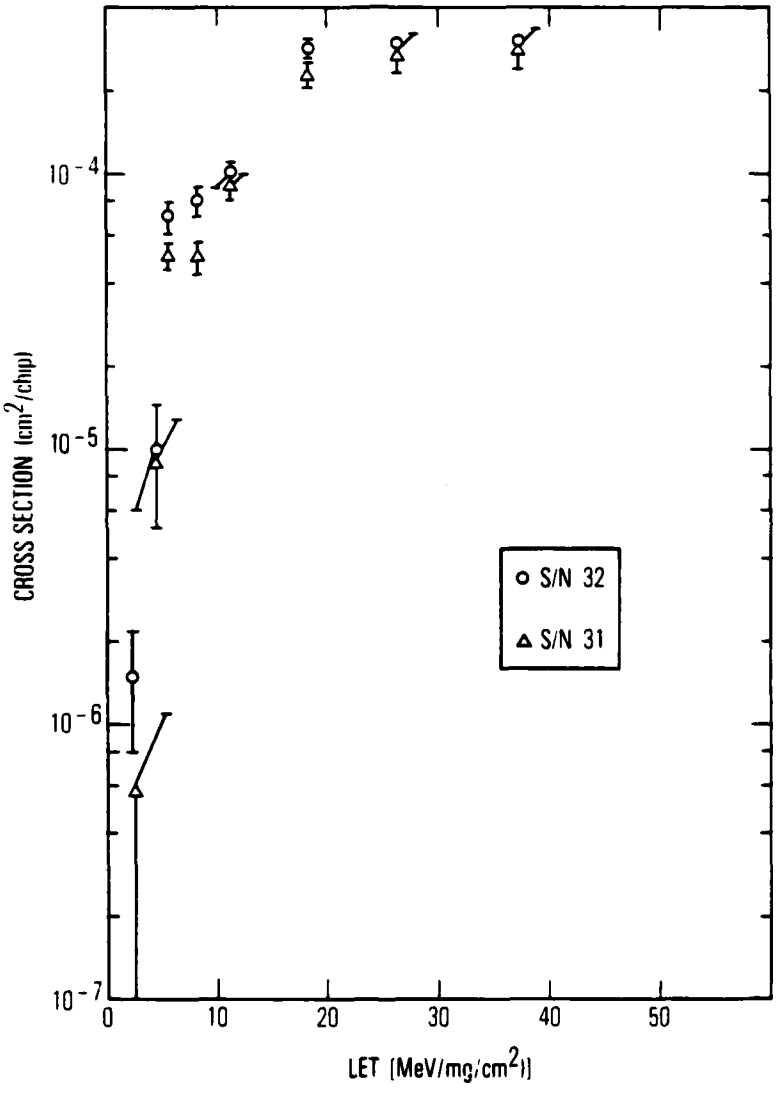
(a)

Figure 5. The Cyclotron Test Results of M6800



(b)

Figure 5. The Cyclotron Test Results of M6800



(c)

Figure 5. The Cyclotron Test Results of M6800

It is very interesting to note that a statistically significant portion of the upset rate is attributable to the ALU. Although this device is a very old one, information about circuit details relevant to the design of the PC and ID has not been available. Therefore, we have tentatively plotted the figure assuming the PCID errors are equally shared among the 16 bits.

So far, it has been worth while to compare the vulnerability of various elements on a "per-bit" basis. Moreover, at the system level, power weights must be assigned to the individual element cross-section, when arriving at an overall system upset cross-section. A simplified approach used in the case of the 6800 is outlined below. The number of user available registers is small (A, B, X, SP and F). We suggest that, on the average, a typical program uses S, PC, and a portion of F registers. The total number of "live and relevant" bits for such a program amounts to about 30. Thus, in first order, we can produce a device-wise cross-section vs LET curve (the "composite" curve) as done for the bit slice as before. Of course, a more precise curve can be obtained, for example, by a Monte Carlo program. We also tested the microprocessor by running the core of a program used by NASA for an actual application. The program ran in a loop that took many steps to arrive at a resultant number whose value was checked by the controller. If correct, the microprocessor would continue in the loop. Upon encountering an error, the controller incremented an external counter and re-initialized the microprocessor. The results of this test are shown in Figure 5c. A strikingly interesting result is that this curve is very close to the composite curve suggested earlier. We realize this similarity corroborates the hypothesis that, in first order, "device-wide" error rate can be calculated using the cross-section vs LET curve in Figure 5c for this device.

C. 80C86 MICROPROCESSOR

The analysis of this device is presented to illustrate the situation where the overall device vulnerability is dominated by the vulnerabilities of the PC and instruction decoder. We tested CMOS/EPI and CMOS/Bulk (the mask number was 1750). The latter device exhibited a high degree of latch-up vulnerability as shown in Figure 6a, and made the soft error upset data

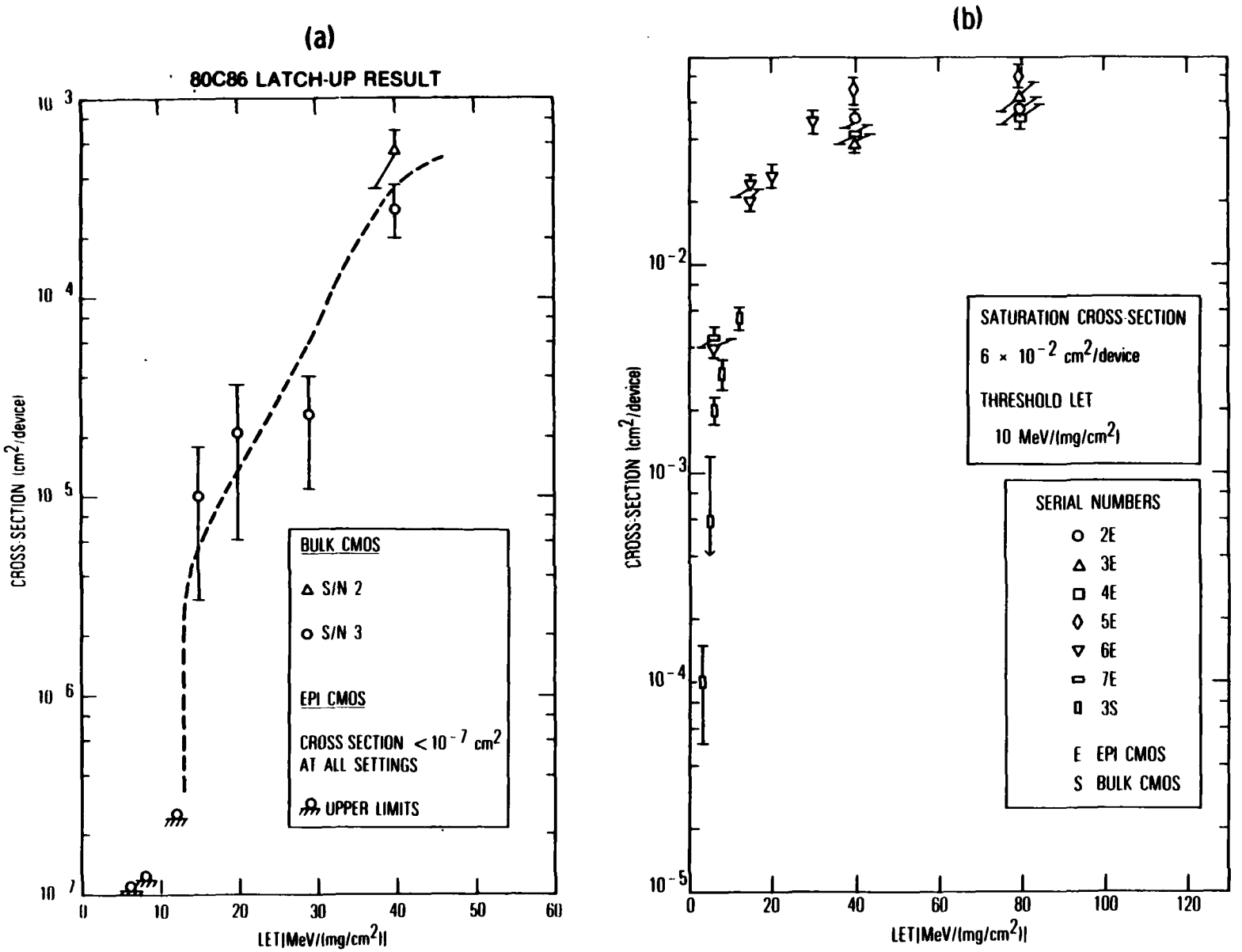


Figure 6. The Cyclotron Test Results of 80C86

collection impossible for LET values beyond 20 MeV/(mg/cm^2). The comparison of SEU cross-sections obtained from various elements showed that the program counter and the instruction decoder were most vulnerable. The composite error rate of the two elements is at least one order of magnitude larger than the combined effect of other registers. Therefore, the cross-section vs LET curve of the device is essentially that of the composite curve of the program counter and the instruction decoder registers as shown in Figure 6b. This curve can be used to obtain the upset rate in terms of error/ device-day.[8,9] Again, it is not proper to use the term "errors/bit-day" in this device in order to predict the upset rate.

The architecture of 80C86 provides very high "performance" because a pipelined architecture is used which allows instructions to be pre-fetched during spare bus cycles. Clearly, this feature is the least desirable from the SEU standpoint, since the longer the instructions stay within the microprocessor registers, the more easily they encounter upset. This device may need a gate level circuit analysis to detect the vulnerable area.

VI. SUMMARY AND CONCLUSIONS

Meaningful test methods for microprocessors are inherently different from methods used for RAMs. This difference carries over to the analysis performed to predict SEU vulnerability. In RAMs, a gate-level analysis, including circuit simulation, is all that is usually needed.[11,12]

Use of this approach, followed by prediction of a microprocessor on a "per-bit" basis, will often lead to an erroneous result.

Even prior to designing a test of a microprocessor, a system level analysis is needed. This is followed by the selection of key functional elements for testing.

Use of the test data entails some degree of reversal of the process, in order to synthesize an "effective" cross-section vs LET curve that can be used to yield meaningful predictions for SEU rates in microprocessors.

REFERENCES

1. C. S. Guenzer, A. B. Campbell, and P. Shapiro, IEEE Trans. on Nucl. Sci., NS-28, 3955, 1981.

2. W. E. Price, J. C. Pickel, T. Ellis, and F. B. Frazee, IEEE Trans. on Nucl. Sci., NS-28, 3946, 1981.

3. P. Shapiro, A. B. Campbell, E. L. Petersen, and L. T. Myers, IEEE Trans. on Nucl. Sci., NS-29, 2072, 1982.

4. W. E. Price, D. K. Nichols, P. R. Measel, K. L. Wahlin, IEEE Trans. on Nucl. Sci., NS-29, 2064, 1982.

5. R. Koga and W. A. Kolasinski, IEEE Trans. on Nucl. Sci., NS-31, 1190, 1984.

6. D. K. Nichols, W. E. Price, C. J. Malone, and L. S. Smith, IEEE Trans. on. Nucl. Sci., 1186, 1984.

7. J. Cusick, R. Koga, W. A. Kolasinski, and C. King, IEEE Trans. on Nucl. Sci., NS-32, 4206, 1985.

8. J. H. Adams, Jr., R. Silberberg, C. H. Tsao, NRL Memorandum Report 4506, 1981.

9. E. L. Petersen, J. B. Langworthy, and S. E. Diehl, IEEE Trans. on Nucl. Sci., NS-30, 4533, 1983.

10. J. A. Zoutendyk, C. J. Malone, and L. S. Smith, IEEE Trans. on Nucl. Sci., NS-31, 1167, 1984.

11. R. L. Johnson, Jr., S. E. Diehl-Nagle, and J. R. Hauser, IEEE Trans. on Nucl. Sci., NS-32, 4122, 1985.

12. J. S. Fu, H. T. Weaver, R. Koga, and W. A. Kolasinski, IEEE Trans. on Nucl. Sci., NS-32, 4145, 1985.

LABORATORY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security projects, specializing in advanced military space systems. Providing research support, the corporation's Laboratory Operations conducts experimental and theoretical investigations that focus on the application of scientific and technical advances to such systems. Vital to the success of these investigations is the technical staff's wide-ranging expertise and its ability to stay current with new developments. This expertise is enhanced by a research program aimed at dealing with the many problems associated with rapidly evolving space systems. Contributing their capabilities to the research effort are these individual laboratories:

Aerophysics Laboratory: Launch vehicle and reentry fluid mechanics, heat transfer and flight dynamics; chemical and electric propulsion, propellant chemistry, chemical dynamics, environmental chemistry, trace detection; spacecraft structural mechanics, contamination, thermal and structural control; high temperature thermomechanics, gas kinetics and radiation; cw and pulsed chemical and excimer laser development including chemical kinetics, spectroscopy, optical resonators, beam control, atmospheric propagation, laser effects and countermeasures.

Chemistry and Physics Laboratory: Atmospheric chemical reactions, atmospheric optics, light scattering, state-specific chemical reactions and radiative signatures of missile plumes, sensor out-of-field-of-view rejection, applied laser spectroscopy, laser chemistry, laser optoelectronics, solar cell physics, battery electrochemistry, space vacuum and radiation effects on materials, lubrication and surface phenomena, thermionic emission, photosensitive materials and detectors, atomic frequency standards, and environmental chemistry.

Computer Science Laboratory: Program verification, program translation, performance-sensitive system design, distributed architectures for spaceborne computers, fault-tolerant computer systems, artificial intelligence, microelectronics applications, communication protocols, and computer security.

Electronics Research Laboratory: Microelectronics, solid-state device physics, compound semiconductors, radiation hardening; electro-optics, quantum electronics, solid-state lasers, optical propagation and communications; microwave semiconductor devices, microwave/millimeter wave measurements, diagnostics and radiometry, microwave/millimeter wave thermionic devices; atomic time and frequency standards; antennas, rf systems, electromagnetic propagation phenomena, space communication systems.

Materials Sciences Laboratory: Development of new materials: metals, alloys, ceramics, polymers and their composites, and new forms of carbon; nondestructive evaluation, component failure analysis and reliability; fracture mechanics and stress corrosion; analysis and evaluation of materials at cryogenic and elevated temperatures as well as in space and enemy-induced environments.

Space Sciences Laboratory: Magnetospheric, auroral and cosmic ray physics, wave-particle interactions, magnetospheric plasma waves; atmospheric and ionospheric physics, density and composition of the upper atmosphere, remote sensing using atmospheric radiation; solar physics, infrared astronomy, infrared signature analysis; effects of solar activity, magnetic storms and nuclear explosions on the earth's atmosphere, ionosphere and magnetosphere; effects of electromagnetic and particulate radiations on space systems; space instrumentation.

...

END

12-86

DTIC